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Figure 6 summarizes these results for V_{gs}=-5V nd two drain biases, showing a greater distribution f leakage currents for increasing drain bias. For the articular TFT geometry and drain doping used in the mulations ($2x10^{19}$ cm^{-3} with an 0.08μm exponential ecay length towards the source), the leakage urrent is at a maximum when the leakage trap is .17μm from the gate edge. The spatial width of the aximum leakage is approximately 0.15μm for $_d$ = 10V and almost a factor of two lower, at 0.08μm, or V_d = 5Volts.

Figure 7 shows the simulated drain bias ependence of the TFT leakage current for three

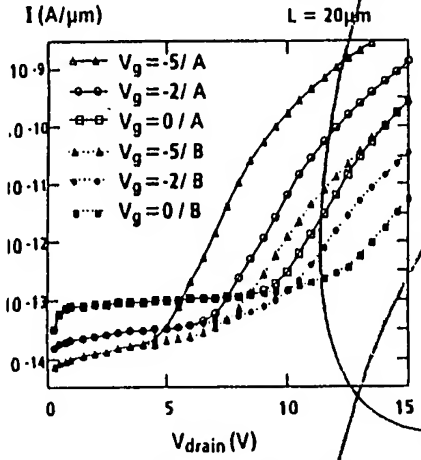

Figure 7. Simulated leakage current versus drain bias for three different gate biasses. The open points, labelled A, correspond to the leakage trap 0.17 μm from the gate edge, while the solid points labelled B, correspond to the leakage trap 0.27 μm from the gate edge.

lifferent gate voltages, from 0V, -2V and -5V, for two lifferent positions of the trap causing leakage urrents. These two trap positions could correspond o two different devices or even the same device with he source and drain terminals reversed [2]. At low $_{ds}$ the leakage current is independent of the eakage trap position, as it is purely determined by he conductance of the poly-Si channel between ource and drain. Whereas in previous work it has een assumed that the leakage at low drain bias is caused by thermionic emission from the source, this mechanism has not been incorporated into our model. At low drain bias our simulations predict that the leakage current is purely a result of drift-diffusion currents in the channel. However, the current is sub-linear with drain bias, as the gate is depleting the channel of majority carriers causing an effective "pinch-off" condition where the current is relatively independent of drain voltage. At high V_{ds} the high field tunneling mechanism becomes dominant, and minority carriers are generated near to the drain, causing device leakage to depend on the position of the traps within the TFT.

Conclusions

In conclusion, for the first time we have successfully simulated the bias, temperature dependence and statistical behaviour of leakage currents in poly-Si TFTs. We have also demonstrated that the activation of the leakage current is determined by the modulation of the barrier to carrier injection near to the TFT source.

The authors would like to thank Prof. Misha Shur from the University of Virginia and their many colleagues at Xerox PARC for valuable discussions.

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ソースドライバ外付けIC方式。但し ICの出力一本に対して ソースバスラインニ本を対応させている。(Fig.6)

SONYは三本を対応。

An LCD Addressed by a-Si:H TFTs with Peripheral poly-Si TFT Circuits

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Abstract

Poly-Si TFTs of an inverted staggered structure are fabricated by peripheral laser annealing of plasma CVD a-Si:H films on SiN gate insulator. The side contact structure improves the TFT characteristics resulting in mobility of 20 cm^2/Vs and on/off ratio of 10^6. The fabrication process, carried out below 300℃, is compatible with conventional a-Si TFT processes. The LCD using a switch matrix of poly Si TFTs has good performance and reduces the number of driver ICs by half.

Introduction

Integration of driving circuits in liquid crystal displays (LCD) addressed by thin film transistors (TFTs) has been investigated for cost reduction and compactness. The polycrystalline silicon (poly-Si) TFT circuits have been applied successfully for small size (~1 inch) LCDs produced by low pressure chemical vapor deposition (LPCVD) processes at high temperatures (>600℃) (1). Larger size (~10 inch) LCDs, however, have been mass-produced with addressing amorphous silicon (a-Si) TFTs without the driving circuits(2). This is because (i) a-Si:H TFTs can be fabricated at low temperatures (<300℃) on cheap glass substrates by plasma CVD (PCVD) processes and (ii) they have a low off-current, ideal for addressing elements. The a-Si:H TFTs have an inverted staggered structure which is totally different from a coplanar structure of conventional poly-Si TFTs. Poly-Si TFTs can be fabricated by laser annealing at low temperatures, but their poor uniformity and high off-current prevents their application for addressing elements.
Based on these points, the concept of a-Si TFT LCDs with poly-Si TFT circuits produced by local laser annealing was proposed on the basis of conventional a-Si:H technology (3).

This paper presents a fabrication method for an inverted staggered poly-Si TFT by excimer laser irradiation on a-Si:H films. A 2.3 inch a-Si:H TFT LCD with poly-Si TFT circuits is fabricated to examine the functionality of the circuits. Effects of the proposed TFT structure on the device performance are also discussed.

Poly-Si TFT Structure and Fabrication

Fig 1 shows a cross sectional view of a poly-Si TFT with the inverted staggered structure. This structure is characterized by undoped double (poly/a) Si layers and an n^+ contact layer on the side wall of the Si layers. The gate electrode is on a glass substrate (Corning 7059). The gate insulator is a multilayer of Al_2O_3, formed by anodic oxidization, and SiN:H, formed by plasma CVD at 300℃. The poly-Si layer (40 nm) is obtained by XeCl excimer laser annealing of a-Si:H deposited by PCVD at 250℃ using monosilane and hydrogen gas. Using such a thin layer ensures thorough annealing to the bottom where the conduction channel will be formed. The annealing is performed at room temperature without preheating because the heating can de-hydrogenate the a-Si films in the addressing area, degrading the characteristics. The standard energy density of the beam is 200mJ/cm^2. The homogenized beam, an 8mm square, is irradiated onto the substrate with a 1mm overlap region between successive pulse beams by moving the substrate stepwise. The upper a-Si (200nm) films are redeposited by PCVD to protect the poly-Si channel against subsequent dry etching of n+ Si. The maximum temperature during fabrication is 300℃ for the gate SiN deposition. A-Si:H TFTs for addressing elements can be fabricated by omitting the laser annealing (a-Si/a-Si layers).

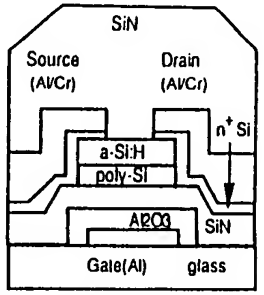

Fig.1 Cross section of poly-Si TFT.

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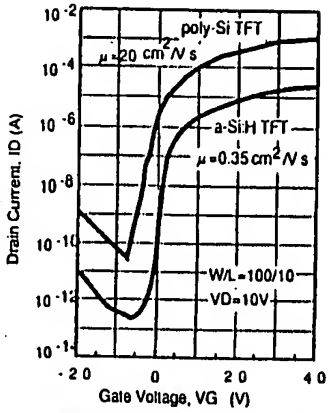


Fig. 2 ID-VG characteristics of TFTs.

Two types of electrode structures were examined. One was the top contact structure as shown in Fig.1 for which the poly/a Si layers were patterned and the phosphorous doped a-Si:H (n+Si) layer and source/drain electrodes were fabricated successively. The other was the side contact structure which had n+Si only on the top of the a-Si layers.

TFT Characteristic

Uniformity

Fig.2 shows drain current (ID)-gate voltage (VG) characteristics of the poly-Si TFT gotten by laser annealing of PCVD film and an a-Si:H TFT formed without annealing. Field effect mobility of the poly-Si TFT is 20cm^2/Vs which is 60 times higher than that of the a-Si TFT. Device performance was measured for 265 TFTs fabricated on a substrate with a 0.3 mm step. Fig 3 shows the mobility distribution for the TFTs. The mobility becomes periodically smaller every 8mm. This periodicity is attributed to the superposition effect of the beam and its energy distribution. Other annealing experiments with different energy densities have shown that once the film is annealed with low energies of about 150 mJ/cm^2 at the beam edge, the mobility can not be improved even by successive 200mJ/cm^2 irradiation.(4) The film annealed with the 150mJ/cm^2 beam is characterized as micro-crystal or amorphous Si with a small amount of hydrogen according to FT-IR and X-ray diffraction methods.

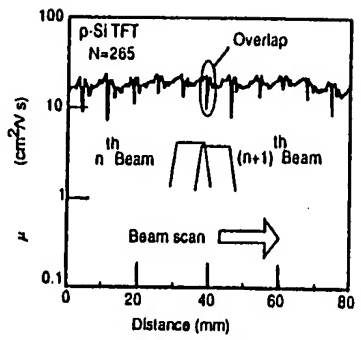


Fig.3 Mobility distribution on substrate (measured using test elements).

TFTs with uniform characteristics can be obtained, except in a 0.6mm strip in the 1 mm overlap regions. The mobility is more than 10cm^2/Vs even in that 0.6mm region, which is high enough for switch matrix elements.

Source and drain electrode structure

Fig.4 shows ID-VG characteristics of TFTs with different source/drain electrode structures. On-state current at a low drain voltage of 0.1V is one order smaller for the top contact structure (dashed line) than that for the side contact structure

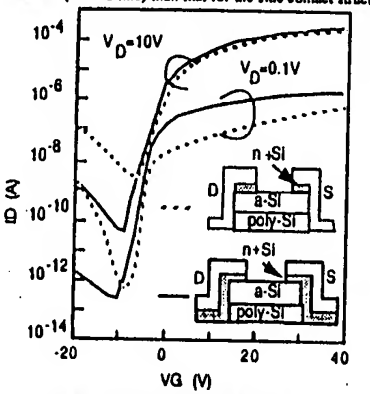


Fig.4 Effect of electrode structure on ID-VG charcteristics.

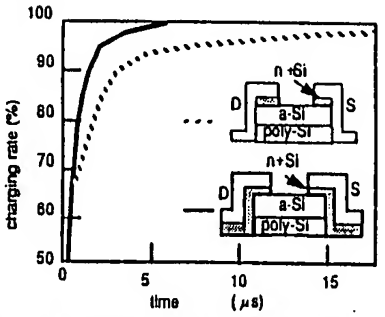


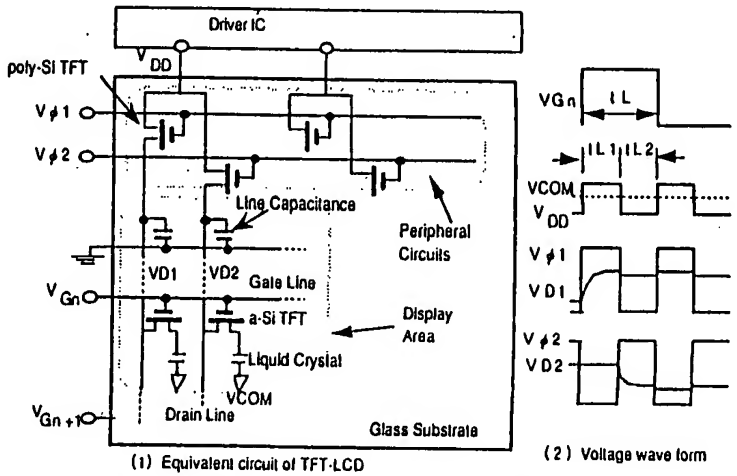
Fig. 5 Charging characteristics of poly-Si TFTs (W/L=1000/10, VG=19V,VD=14V,C=90pF).

(solid line). This is due to the series resistance between the electrode and the conduction channel in the poly-Si. Presumably, native oxide at the a-Si/poly-Si interface formed at the time of air exposure between the two steps of Sideposition. Current in the top contact structure must flow out from the channel poly-Si across the resistive native oxide to the drain electrode. In the side contact TFT, the current can flow out directly to the electrode resulting in higher values of the current. This side contact structure can also improve the off state characteristics. The current in the side contact structure is smaller than that of the top contact structure by several orders. This is because the holes can be blocked by the n$^+$Si layer at the side contact while they can be injected freely into the drain metal in the top contact structure. The on/off current ratio of the side contact structure TFT is as high as 10^6.

The charging characteristics were measured with a load capacitance equivalent to the drain line capacitance in a large LCD. They are shown in Fig.5. The capacitance can be charged by the TFT in 7 μs which is one fifth of the gate addressing time in pixels for VGA type LCDs.

a-Si:H TFT LCD with poly-Si TFT circuits

Fig 6 shows a schematic of the a-Si:H TFT LCD with an array of poly-Si TFTs which can halve the number of the drain driver ICs. The poly-Si TFTs connect each output terminal of the driver IC to two drain lines in the pixel area. The signal voltages for the two lines are supplied successively while a pixel gate line is selected. No interconnection points



(1) Equivalent circuit of TFT-LCD

(2) Voltage wave form

Fig.6 Schematic of peripheral circuit (50% reduction in number of driver ICs).

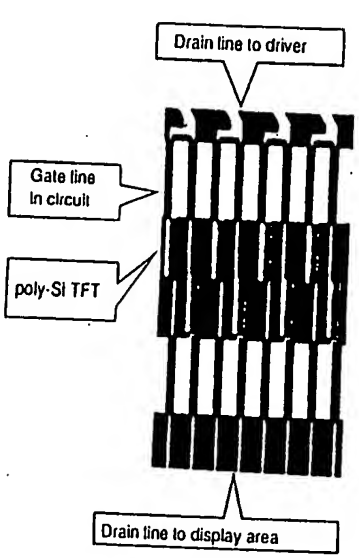


Fig.7 Photograph of fabricated circuit.

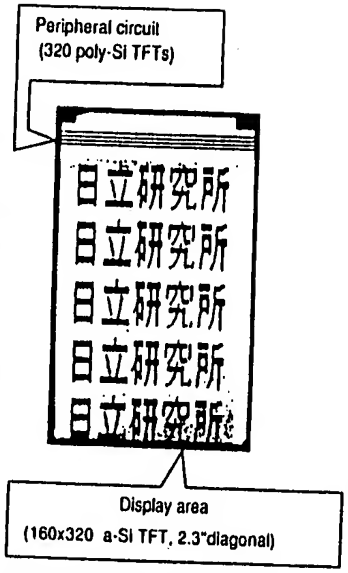


Fig.8 Displayed image of prototype LCD.

are needed between gate and drain lines in the circuit. The array consists of only n-ch poly-Si TFTs. Therefore the LCD can be fabricated on the basis of conventional a-Si:H TFT technologies with only laser annealing applied to the circuit area.

Fig. 7 shows a photograph of the poly-Si TFT circuit fabricated. Fig. 8 is a displayed image in the 2.3 inch LCD addressed by a-Si TFTs with the poly-Si TFT array. It has good uniformity in the display area and sharp contrast between adjacent pixels, confirming functionality of the circuits. Further reduction of IC number can be expected thanks to the high-speed charging (Fig.5) by simply increasing the number of lines connected to each terminal of the driver ICs.

Summary

A 2.3 inch a-Si:H TFT LCD with a switch matrix of poly-Si TFTs has been developed and fabricated with all steps carried out below 300°C. The poly- Si TFTs have an inverted staggered structure with poly-Si and a-Si double layer. The side contact structure of the TFTs improves the on- and off-state characteristics significantly. The process, using PCVD and XeCl laser annealing, is closely compatible with the mass-production processes of large size a-Si TFT LCDs.

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A NOVEL FLOATING GATE SPACER POLYSILICON TFT

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Abstract

This paper reports on a new polysilicon TFT device utilizing a polysilicon floating gate spacer (FGS) to reduce the OFF-state leakage current and suppress the kink effect while maintaining a reasonable ON current. The new device has demonstrated a better ON/OFF current ratio than both conventional non-LDD TFT devices and LDD devices with oxide spacers. The device structure is simple and self-aligned. The FGS concept applies to both active matrix liquid crystal displays (AMLCD) and SRAM applications.

Introduction

Polysilicon TFTs have been widely used in active matrix liquid crystal displays (AMLCD) and SRAM applications. One of the major problems of these TFTs is the OFF-state leakage current, which causes charge loss in LCDs and high standby power dissipation in SRAMs. The main mechanism for the leakage current generation has been identified as field emission via grain boundaries caused by the high electric field at the drain [1]. Experimental data and simulation show the strong dependance of leakage current on the drain field [2]. Conventional LDD structures [3] and Offset Drain structures [4] have been used to reduce the drain field, thereby reducing the leakage current. However, these structures also significantly reduce the ON current due to the extra series resistance introduced. We have successfully developed a new LDD structure using polysilicon floating gate spacer (FGS) technology to solve this problem.

Device Structure

The structures of the FGS device, the oxide spacer LDD device, and the non-LDD device are shown in Fig. 1. In the FGS device, the polysilicon side-wall spacer is isolated from the gate by a thin deposited oxide (200Å), and acts like a floating gate. The floating gate potential is determined by both the gate voltage and the drain voltage through capacitive coupling. In the OFF state (V_D=Vdd, V_G=0), the intermediate potential on the floating gate at the drain side reduces the vertical field between the drain and the gate. The lateral drain field is reduced by having the drain away from the gate edge and/or by the gradual change in the lateral doping profile if an LDD implant is performed. In the ON state (V_G>0), the floating gate potential results in an accumulation layer under the spacer (LDD region), thereby lowering the series resistance of both the source side and the drain side.

MEDICI simulation results comparing the three types of devices show that the maximum OFF state electric field for the FGS device is approximately half of the non-LDD device and roughly the same as the oxide spacer LDD device (Fig. 2), which indicates that the leakage in both the FGS device and the oxide spacer device should be smaller than in the non-LDD device. However, in the ON state, the electron density in the LDD region is two orders of magnitude higher in the FGS device than in the oxide spacer device (Fig. 3), which implies that the ON current will be significantly larger in the FGS device than in the oxide spacer device.

Device Fabrication

We have fabricated the polysilicon NMOS FGS TFT along with the oxide spacer TFT, and the conventional non-LDD TFT, using a low temperature process. The main processing steps for the FGS TFT devices are illustrated in Fig. 4.

Silicon wafers with 5000Å thermally grown oxide were used as starting substrates. A 1100Å thick Si channel layer was deposited at 550°C in amorphous form by low-pressure chemical vapor deposition (LPCVD). The a-Si film was then crystallized during a 20-hour anneal in Ar at 600°C. The crystallization was verified by X-ray diffraction (XRD). After the definition of polysilicon islands, 500Å of gate oxide was deposited by LPCVD at 400°C, and subsequently densified at 600°C in O_2 for 10 hours, and then in N_2 for 2 hours. The gate polysilicon was deposited and patterned. Some wafers were subjected to an LDD implant with doses of $1x10^{13}cm^{-2}$ or $5x10^{13}cm^{-2}$. For the FGS devices, a thin oxide (200Å) was deposited, followed by a 5500Å side-wall polysilicon deposition. For the oxide spacer devices, a 5400Å oxide was deposited. Side-wall spacer etch was then performed for the FGS devices and the oxide spacer devices separately. The non-LDD devices were not subjected to the LDD implant and the side-wall deposition/etching. After a self-aligned source/drain/gate implant (As+, $1x10^{15}cm^{-2}$), the isolation oxide was deposited. The dopants were activated during a 600°C Ar anneal for 1.5 hours. The isolation oxide also acted as a cap to prevent the dopants from out-diffusion during activation anneal. Contact lithography and contact etch were then carried out. Finally, aluminum was deposited and defined, followed by a forming gas anneal at 400°C for 45 minutes.

The key processing conditions for the FGS TFT devices are summarized in Table I:

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Chapter 9 Analog Switching Circuits

9.1 Fundamentals, p. 46, ll. 6-11

A CMOS switch, in which a pair of complementary transistors is connected in parallel with each other so as to be turned ON simultaneously, is effectively applicable as shown in FIG. **9.1(b)**. FIG. **9.1(b)** also shows a relationship between the input voltage and the conductance of the switch. Either the PMOS transistor or NMOS transistor operates as shown in FIG. **8.29** to charge or discharge the capacitor to the input voltage level. Accordingly, the conductance of the switch in ON state is sufficiently large irrespective of its input voltage. In addition, its output voltage is equal to its input voltage thereof.